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DESIGN AND COMPARATIVE ANALYSIS OF 6T SRAM BITCELL USING 45NM, 90NM AND 180NM TECHNOLOGY

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***Abstract*—**SRAM has good storage density and fast access time which made it a crucial component in VLSI chips. Due to its ease in usage, minimal standby leakage, SRAM's are widely used in many

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applications. The recent demands for highly secure and reliable user systems made it useful everywhere in recent times not only in communication applications but also in Transportation applications, Industrial applications, Medical/Healthcare applications, Automobile applications etc.. A CMOS SRAM cell uses less power and requires less read and write time. This study uses a 6T SRAM cell that consumes less power, space and time to read and write data. SRAM is a type of random-access memory, which stores data for longer duration without refreshing the circuits. In this paper the performance analysis of 6T SRAM in 180nm, 90nm and 45nm technology in terms of write time (propagation delay) using cadence tool is studied. The aim is to develop a 6T SRAM design which yield less delay because most of the area on memory chip is consumed by SRAM cell.

***Keywords*—**SRAM, VLSI, 6T(Transistor) technology, write time, delay

I. INTRODUCTION

Now-a-days technology is increasing and latest equipments are introduced, where most of the inventions are related to Electronics. Every IC (Integrated Circuit) is made up of many components such as I/O's, CPU's, Memory, etc.., depending on the applications and requirements. These new inventions bring many advantages in terms of functionality, ease of use, improved performance etc.., Memory is of different types such as RAM (Random Access Memory), ROM (Read Only Memory), Cache Memory. RAM is a volatile memory whereas ROM is non-volatile memory. RAM is divided into SRAM & DRAM. ROM is classified as Mask ROM, EPROM (Erasable Programmable ROM), EEPROM (Electrically Erasable Programmable ROM), Flash memory. Cache Memory is of L1 cache, L2 Cache, L3 Cache. All these classifications have their own uses & characteristics. SRAM, which stands for Static Random Access Memory, is a type of volatile semiconductor memory that is used in various electronic devices such as computers, smart phones, and networking equipment. Unlike Dynamic Random Access Memory (DRAM), which requires periodic refreshing to maintain data, SRAM can hold data as long as power is supplied to the system[1-4].

SRAM can be designed using BJT's and also MOSFET's. In BJT's, switching power loss is larger, so MOSFET's are widely used as its switching power loss is reduced. A semiconductor device can be considered as a kind of resistor that generates heat in proportion to the ON resistance as current flows through it. While designing a device, need to check both forms of power static power & dynamic power. Static power, also known as leakage power or standby power, static power consumption refers to the power dissipated by a device or circuit even when it's not actively switching or performing any computation. Dynamic power, on the other hand, is the power dissipated by a device or circuit during its active operation, primarily due to the charging and discharging of capacitances when transistors switch states[5-9].

Nanotechnology is a field of science and engineering that deals with the manipulation of matter on an atomic or molecular scale, typically ranging from 1 to 100 nanometers. At this scale, materials often exhibit unique properties and behaviors that are distinct from those at larger scales. "Nanotechnology" in the context of semiconductor manufacturing refers to the process

technology node used to fabricate integrated circuits (ICs). It represents the minimum feature size of the transistors and other components on a chip. Nanotechnology is often referred to by its technology node, such as 180nm, 90nm, 65nm, 45nm, 32nm, 22nm, 14nm, 10nm, 7nm, and so on."Nanotechnology is crucial for the development of advanced electronic devices, including microprocessors, memory chips, graphics processing units (GPUs), and system-on-chip (SoC) designs. Applications of SRAM in nanotechnology are Memory devices, cache memory, logic gates and circuits, Neuromorphic Computing, Automobiles, Medical instruments etc.., The technology advancements contribute to improvements in the performance, power efficiency, and functionality of electronic devices. This paper contains different sections explaining about design of SRAM[10-14].

Section I: Contains the introduction of SRAM Memory, Nanotechnology and various applications of SRAM in Nanotechnology.

Section II: Involves the literature survey which is mainly carried out in order to analyze the background of the current work which helps to find out flaws in the existing system and guides on which the problems can be resolved.

Section III: Includes the working of SRAM 6T bitcell and its operations. It also shows the schematic of 6T bitcell.

Section IV: It Involves analysis of various parameters, calculations and waveforms that are simulated using cadence virtuoso.

Sections V: Results are compared and concluded in various technologies.

II. LITERATURE SURVEY

In this work, the 6T SRAM bitcell circuit is designed with 7nm Technology and compared with 45nm Technology. In this work, various operations of bitcell such as HOLD state, Read Operation for reading of 0 & 1, Write Operation for writing of 0 & 1 are explained and also analyzed various parameters like delay, power etc.,. The stability criteria of 6T SRAM bitcell is mainly concerned since most of the area in memory chip is consumed by SRAM. The power dissipation, delay, and transient response are analyzed through various procedural calculations[3]. In this work, SRAM circuits for 6T SRAM bitcell are designed in 45nm, 7nm technologies using cadence virtuoso. The detailed explanation of hold, read and write operations of each SRAM 6T bitcell is mentioned and transient responses are also shown. The basic inverter operation and working, 6T SRAM circuit schematic in 45nm technology and working operations are explained. The scaling down of CMOS transistors is associated with leakage currents causing reduced performance. In today's culture, power consumption is a significant

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problem for electronic gadgets. Consequently, the primary goal is to reduce the amount of power that SRAM cells consumes. This work illuminates and analyzes SRAM with various cell designs and elaborates on SRAM with 6 transistors, its operation, performance analysis, and simulation[7].

III. PROPOSED METHODOLOGY

Figure 1 shows the 6T SRAM Bitcell circuit diagram. Here M_1, M_3 are PMOS transistors & M_2, M_4, M_5, M_6 are NMOS transistors. In the bitcell, the M_1-M_2 & M_3-M_4 pairs are a cross-coupled CMOS inverters which gives stability to the bitcell. M_5&M_6 are access transistors. These access transistors are connected to Bitlines and controlled by Wordlines.

This bitcell operates in 3 different modes.

a) Hold mode
b) Read mode
c) Write mode

a) Hold mode:

This mode holds the value that is present inside the bitcell.

When WL=0(LOW), then the access transistors are deactivated. Due to this, Q & Qbar will hold the current value that already exists. Hence the bitcell will be in "HOLD" state.

b) Read mode:

This mode reads the value that is present inside the bitcell.

When WL=1(HIGH), then the access transistors are turned ON. If Q=1 & Qbar=0, then the respective values of Q &Qbar are passed through access transistors resulting the reading of the values in respective Bitlines (BL, BLbar).

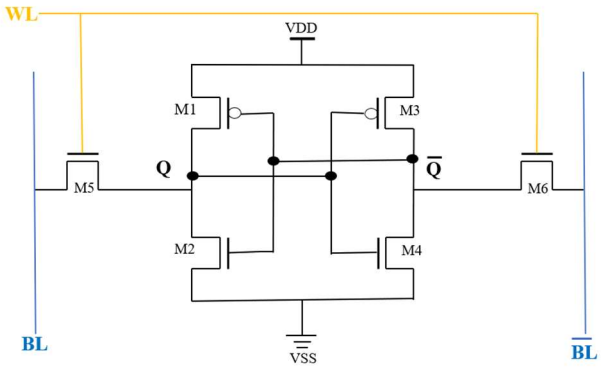

Figure1: Circuit diagram of 6T SRAM Bitcell

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- **Operation:**

In READ operation, Initially both the bitlines (BL, BLbar) are precharged to V_{DD} (HIGH). When the WL is HIGH, access transistors are turned ON & the values of Q & Qbar are passed through the access transistors. If the value of Q=1 & Qbar=0, then the BL remains to read the value as '1'and BLbar starts discharging to '0' since the access transistor passes the Qbar value i.e '0' to BLbar. Hence, thereby reading '0' & '1' through bitlines.

c) Write mode:

This mode writes the values that are given externally through bitlines from '0' to '1' (or) '1' to '0'inside the bitcell. When WL=1(HIGH), then the access transistors are turned on. The value that is to be written inside bitcell is given through the bitlines. If BL=0, BLbar=1 then the respective values inside a bitcell will be written from Q='1' to Q='0'. Similarly, from Qbar='0' to Qbar='1' resulting the writing inside bitcell.

- **Operation:**

In WRITE operation, Initially if Q=1 & Qbar=0, then the bitlines are given as BL='0' & BLbar='1'. When WL is HIGH, access transistors are turned ON & as BLbar=1, this value passes through access transistor M_6. This acts as input to the inverter pair M_1-M_2.
The output will be '0' i.e Node 'Q' will be now changed from '1' to '0'. This acts as input to the inverter pair M_3-M_4, leading to output at Node 'Qbar' written from '0' to '1'. Finally, the values are Q=0 & Qbar=1.

Strengths of Pull-Up(PU), Pull-Down(PD) & Pass-Gate(PG)/Access Transistors:

In read operation, PD & PG transistors play a vital role to pass the values that are present inside the bitcell. So, to stabilize the value inside the bitcell, the pre-charged bitlines should not distort the values through PG. Hence, the strength of the PG should be less than PD. So, width of PD>PG in the range of 1.5 to 2.5 times (Approximately considered as W_{PD}~=$2W_{PG}$).

In write operation, PU & PG transistors play a crucial role in writing the values that are given through the bitlines. So, to pass the values through access transistors the strength of PG should be greater than PU. So, width of PG>PU in the range of 1.2 to 1.5 (Approximately considered as W_{PG}~=$1.5W_{PU}$).

Hence, with the above mentioned ratios for the widths of PU, PD and PG makes the stable read and write operations without any distortions.

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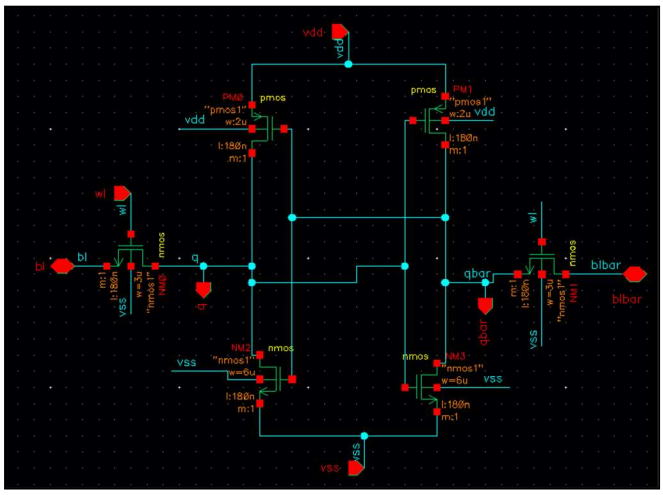

Figure 2: Schematic of 6T SRAM bitcell using 180nm technology

The Figure 2 is the schematic representation of 6T SRAM bitcell using 180nm technology, where widths are taken as W_{PU} =2µm, W_{PG} = 3µm & W_{PD} = 6µm. These implements the stable hold, read and write operations as detailed above.

Figure 3 shows the test bench that is considered, where WL pulse signal varies from 0v to 1v (pulse width =10nsec, period =15nsec) & BL pulse varies from 0v to 1v and BLbar pulse varies from 1v to 0v (pulse width = 2nsec, period = 4nsec). V_{DD} is DC voltage calculated with 0.8v, 1v and 1.2v. V_{SS} is grounded with 0v.

The Figure 4 is the schematic representation of 6T SRAM bitcell using 90nm technology, where widths are taken as W_{PU} =120nm, W_{PG} = 180nm & W_{PD} = 360nm. These implements the stable hold, read & write operations as detailed above.

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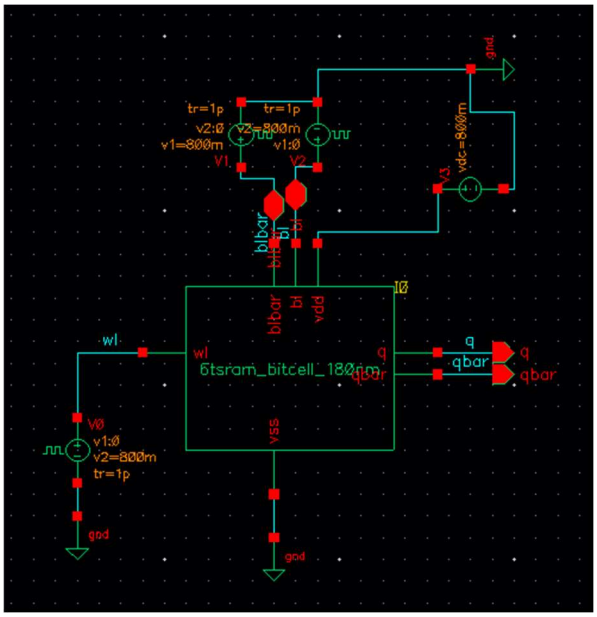

Figure 3: Test Bench of 6T SRAM bitcell using 180nm technology

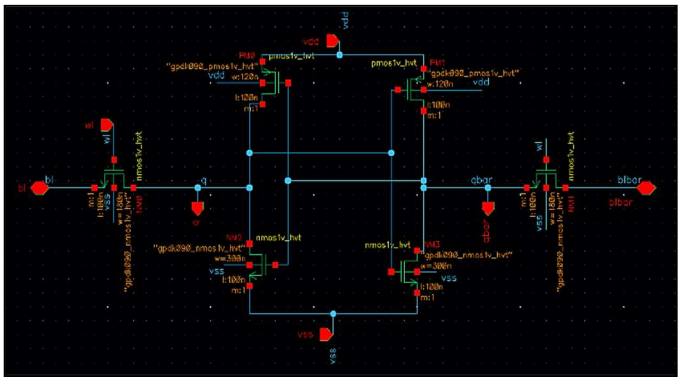

Figure 4: Schematic of 6T SRAM bitcell using 90nm technology

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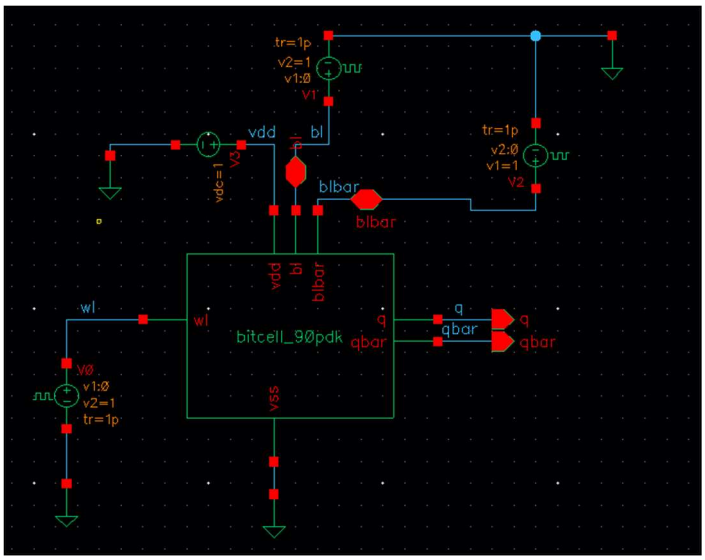

Figure 5: Test Bench of 6T SRAM bitcell using 90nm technology

Figure 5 shows the test bench that is considered, where WL pulse signal varies from 0v to 1v (pulse width =10nsec, period =15nsec) & BL pulse varies from 0v to 1v and BLbar pulse varies from 1v to 0v (pulse width = 2nsec, period = 4nsec). V_{DD} is DC voltage operated with 0.8v, 1v and 1.2v. V_{SS} is grounded with 0v.

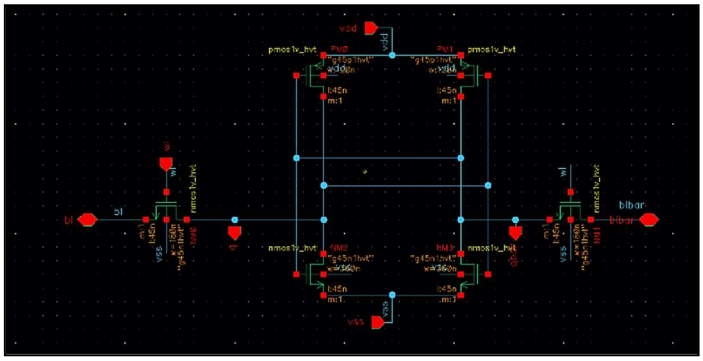

Figure 6: Schematic of 6T SRAM bitcell using 45nm technology

The Figure 6 is the schematic representation of 6T SRAM bitcell using 45nm technology, where widths are taken as W_{PU} =120nm, W_{PG} = 180nm and W_{PD} = 360nm. These implements the stable hold, read and write operations as detailed above.

Figure 7 shows the test bench that is considered, where WL pulse signal varies from 0v to 1v (pulse width =10nsec, period =15nsec) and BL pulse varies from 0v to 1v and BLbar pulse varies from 1v to 0v (pulse width = 2nsec, period = 4nsec). V_{DD} is DC voltage operated with 0.8v, 1v and 1.2v. V_{SS} is grounded with 0v.

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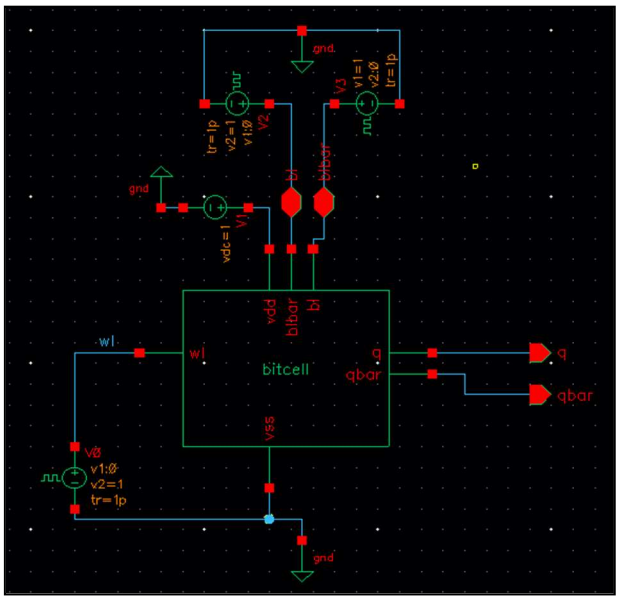

Figure 7: Test Bench of 6T SRAM bitcell using 90nm technology

IV. SIMULATION RESULTS AND DISCUSSION

The 6T SRAM Bitcell is designed using cadence virtuoso tool with 180nm, 90nm & 45nm technology files. The parameters like transient analysis and DC power analysis are calculated for various technologies i.e 180nm, 90nm, 45nm. These parameters are compared across all technologies. The waveforms are depicted to compare the propagation delay of writing the values of Q & Qbar from '0' to '1' & from '1' to '0' across technologies.

Waveforms in Figure 8 are plotted for WL, BL, BLbar, where WL pulse signal varies from 0v to 1v (pulse width =10nsec, period =15nsec), BL pulse varies from 0v to 1v and BLbar pulse varies from 1v to 0v (pulse width = 2nsec, period = 4nsec). V_{DD} is DC voltage operated with 1v. V_{SS} is grounded with 0v. The outputs resulted are Q & Qbar. Here BL and BLbar are compliments of each other. Based on these inputs the outputs Q & Qbar stores the values by either read or write operation accordingly.

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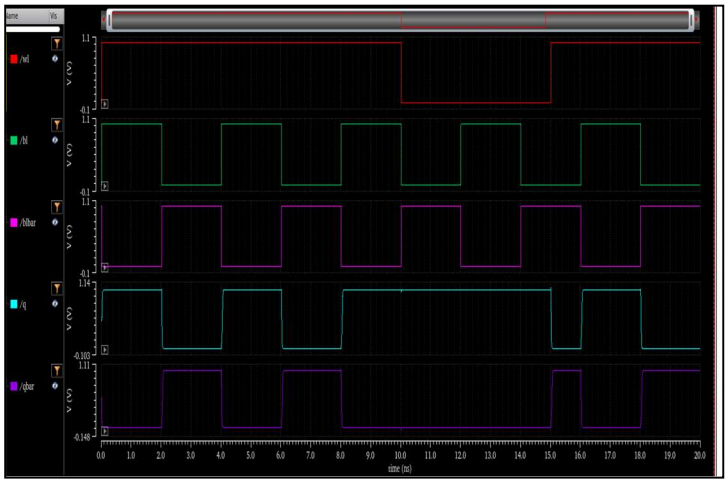

Figure 8: Waveform for Transient Analysis of Write Operation in 6T SRAM Bitcell in 45nm Technology

The similar operation is performed on 90nm technology & 180 nm technology and the waveforms are plotted in Figure 9 and Figure 10 respectively.

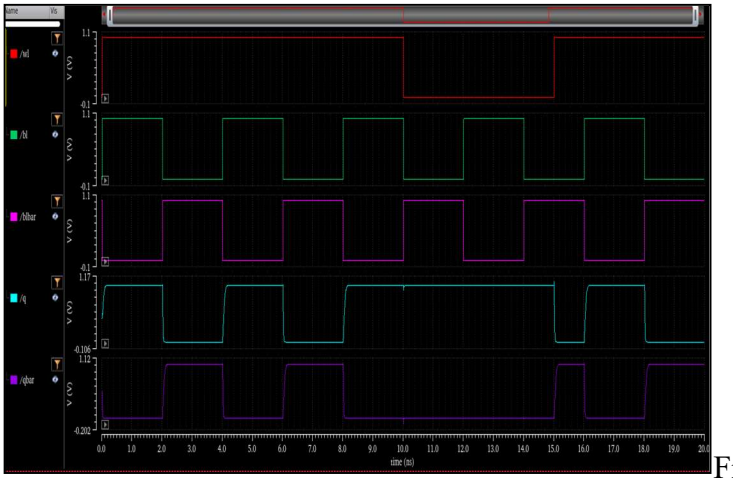

Figure 9: Waveform for Transient Analysis of Write Operation in 6T SRAM Bitcell in 90nm Technology

Here analysis is done with two types of simulations:

1. Transient analysis

Propagation Delay: Propagation Delay is defined as the time taken for the signal to reach from low(0) to high(1) or high(1) to low(0).

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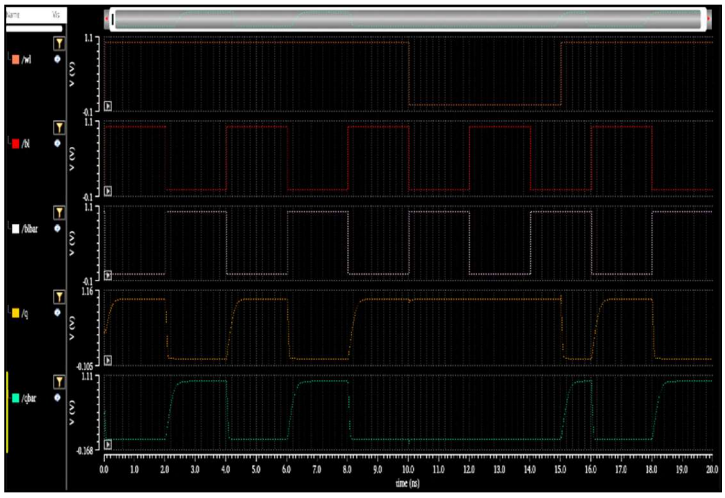

Figure 10: Waveform for Transient Analysis of Write Operation in 6T SRAM Bitcell in 180nm Technology

There are write delay and read delay in 6T SRAM bitcell. Write delay is the time required for writing 0 or 1 to the storage node (Q/Qbar) from the time word line is activated. Read delay is the time when BL/BLbar is discharged from its initial high level from the time wordline is activated.
Here write delay is calculated which is defined as the time taken for the BL/BLbar to write the stored value at node Q/Qbar from '0' to '1' or '1' to '0'.
From the waveforms shown, write delay is calculated for BL & BLbar at different supply voltage levels(V_{DD}) i.e. 0.8v,1.0v and 1.2v, where WL pulse signal varies from 0v to 1v (pulse width =10nsec, period =15nsec, rise time(tr)=1ps, fall time(tf)=1ps) and BL pulse varies from 0v to 1v and BLbar pulse varies from 1v to 0v (pulse width = 2nsec, period = 4nsec, rise time(tr)=1ps, fall time (tf)=1ps).

Write Delay calculated in 180nm Technology for 6T SRAM Bitcell:

- For 0.8v:

  propagation delay in writing from '1' to '0' = 0.51ns
  propagation delay in writing from '0' to '1' = 0.88ns
- For 1.0v:

  propagation delay in writing from '1' to '0' = 0.255ns
  propagation delay in writing from '0' to '1' = 0.5ns
- For 1.2v:

  propagation delay in writing from '1' to '0' = 0.166ns
  propagation delay in writing from '0' to '1'' = 0.358ns

Write Delay calculated in 90nm Technology for 6T SRAM Bitcell:

- For 0.8v:

  propagation delay in writing from '1' to '0' = 0.1513ns

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propagation delay in writing from ‘0’ to ‘1’ = 0.216ns

- For 1.0v:

propagation delay in writing from ‘1’ to ‘0’ = 0.0912ns
propagation delay in writing from ‘0’ to ‘1’ = 0.1403ns

- For 1.2v:

propagation delay in writing from ‘1’ to ‘0’ = 0.067ns
propagation delay in writing from ‘0’ to ‘1’ =0.119ns

Write Delay calculated in 45nm Technology for 6T SRAM Bitcell:

- For 0.8v:

propagation delay in writing from ‘1’ to ‘0’ = 0.15ns
propagation delay in writing from ‘0’ to ‘1’ = 0.1942ns

- For 1.0v:

propagation delay in writing from ‘1’ to ‘0’ = 0.062ns
propagation delay in writing from ‘0’ to ‘1’ = 0.082ns

- For 1.2v:

propagation delay in writing from ‘1’ to ‘0’ = 0.0378ns
propagation delay in writing from ‘0’ to ‘1’ = 0.0477ns

Here, it is observed that with the increase in supply voltage the delay is increased. Also the time taken to write from ‘0’ to ‘1’ is greater than the time taken to write from ‘1’ to ‘0’. This is because to result 0 the bitlines discharges easily compared to charging of bitlines to 1 by writing 0 using PMOS pull-up transistor.

2. DC Power Analysis

DC power analysis is done to calculate the circuit biasing points over range of values. It computes DC working points. Analysis is done with respect to Figure 11, Figure 12 and Figure 13 in 45nm, 90nm and 180nm technologies respectively

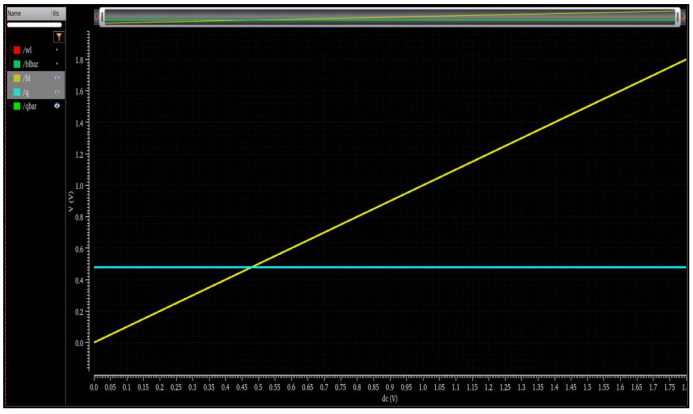

Figure 11: DC power Analysis of 6T SRAM

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Bitcell in 45nm Technology

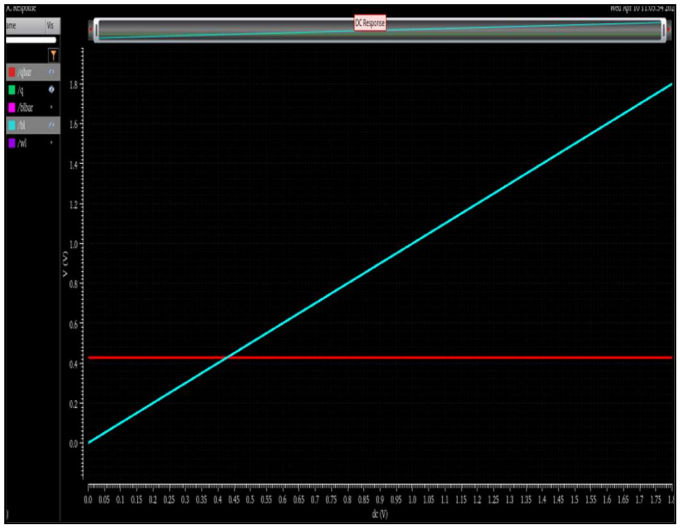

Figure 12: DC power Analysis of 6T SRAM Bitcell in 90nm Technology

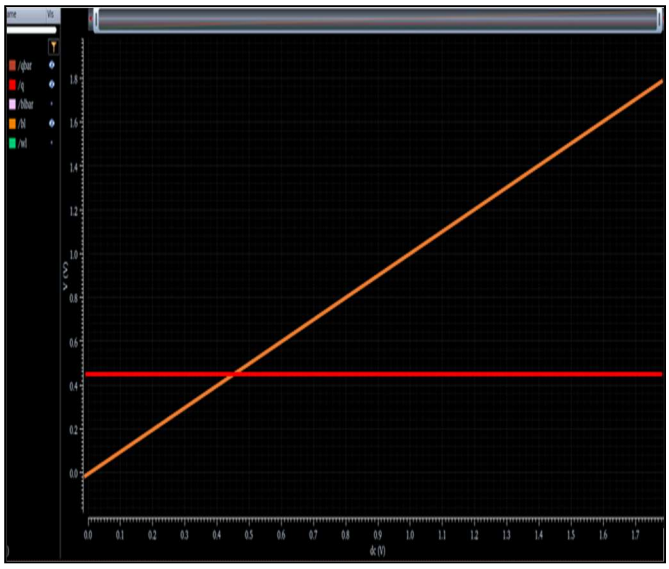

Figure 13: DC power Analysis of 6T SRAM Bitcell in 180nm Technology

Below Tables I and II shows the comparison of various parameters in 180nm, 90nm and 45nm technologies. The results depicts that the propagation delay (write time), DC power in various technologies. Here the trend is observed from the simulation results implies that, as technology scales down, delay in the circuits will be reduced that means the speed of the circuit will be more which means the read time, write time, access time will be less. Also, the delay increases with the increase in supply voltage.

TABLE I COMPARISION OF VARIOUS PARAMETERS WITH SUPPLY VOLTAGE IN 180nm TECHNOLOGY

Write time(propagation delay)	Supply Voltage(V_{DD})		
	0.8v	1.0v	1.2v
Write time from '1' to '0'	0.51ns	0.255ns	0.166ns
Write time from '0' to '1'	0.88ns	0.50ns	0.358ns

TABLE 2 COMPARISION OF VARIOUS PARAMETERS WITH SUPPLY VOLTAGE IN 90nm TECHNOLOGY

Write time(propagation delay)	Supply Voltage(V_{DD})		
	0.8v	1.0v	1.2v
Write time from '1' to '0'	0.1513ns	0.0912ns	0.067ns
Write time from '0' to '1'	0.216ns	0.1403ns	0.119ns

TABLE 3 COMPARISION OF VARIOUS PARAMETERS WITH SUPPLY VOLTAGE IN 45nm TECHNOLOGY

Write time(propagation delay)	Supply Voltage(V_{DD})		
	0.8v	1.0v	1.2v
Write time from '1' to '0'	0.15ns	0.062ns	0.0378ns
Write time from '0' to '1'	0.1942ns	0.082ns	0.0477ns

V CONCLUSIONS

In this work, 6T SRAM cell in 180nm and 45nm technology using cadence virtuoso is designed. The 6T SRAM is studied in detail which lets to know its internal operation. The schematic, test circuit is designed and is analyzed with different input values and verified with Transient, DC Response and calculated various parameters like write delay in the circuit of transitioning from high to low and low to high by following various procedural calculations. It is observed that performance of 6T SRAM in 45nm technology is better than that in 90nm & 180nm in terms of these parameters. As the speed, performance is increased, due to this the leakage currents will be increased this results in some precharging or leakage controlling circuits additionally. Also the area is reduced since the width of the transistors is reduced almost to half. From the above analysis, it is observed that as technology scales down, the power, write delay gets reduced and as the supply voltage is increased, the write time is reduced since the stability is reaching earlier hence the data can be written faster. Thus concluded that by approaching the latest nm technologies like 45nm, 32nm, 22nm and 10nm can get more space in architecture by reducing width of transistors. The future scope is generating memory cells in order of mega, giga, terabytes that can be designed and analyzed further. SRAM usage has been increasing since it is growing its application in automobile industries, medical fields, aerospace,

networking etc..,

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